In the Claims

1. (ORIGINAL) A method for operating a system comprising an Asynchronous Transfer Mode Segmentation and Re-assembly (SAR) connected to a host, the method comprising:

writing from the SAR to the host to indicate where the SAR is reading from a SAR queue;

writing from the host to the SAR to indicate where the host is reading from the host queue;

transferring information between the host queue and the SAR queue; and

transferring a first cell payload between the host and the SAR in response to transferring the information.

2. (ORIGINAL) The method of claim 1 further comprising:

writing from the SAR to the host to indicate where the SAR is writing to the host queue; and

writing from the host to the SAR to indicate where the host is writing to the SAR queue.

3. (ORIGINAL) The method of claim 2 further comprising:

controlling the SAR queue to indicate if the information in the SAR queue has been processed; and

controlling the host queue to indicate if the information in the host queue has been processed.

4. (ORIGINAL) The method of claim 3 wherein:

transferring the information comprises writing a first pointer from the host to the SAR queue; and

transferring the first cell payload comprises reading a first cell payload from a first buffer in the host in response to the first pointer in the SAR queue.

5. (ORIGINAL) The method of claim 4 wherein reading the first cell payload from the host in response to the first pointer in the SAR queue comprises activating a first SAR buffer descriptor in response to the first pointer in the SAR queue and reading the first cell payload from the first buffer in the host in response to activating the first SAR buffer descriptor.

6. (ORIGINAL) The method of claim 5 wherein the first SAR buffer descriptor is associated with the first buffer in the host and the first pointer indicates the first SAR buffer descriptor.

7. (ORIGINAL) The method of claim 6 further comprising:

activating a second SAR buffer descriptor in response to reading the first cell payload from the first buffer in the host; and

reading a second cell payload from a second buffer in the host to the SAR in response to activating the second SAR buffer descriptor.

8. (ORIGINAL) The method of claim 4 further comprising writing a second pointer from the SAR to the host queue in response to transferring the first cell payload to the SAR to indicate that transfer of the first cell payload is complete.

9. (ORIGINAL) The method of claim 8 wherein the second pointer indicates a first host buffer descriptor that is associated with the first buffer.

10. (ORIGINAL) The method of claim 9 further comprising mirroring the first host buffer descriptor and the first SAR buffer descriptor.

11. (ORIGINAL) The method of claim 3 wherein:

transferring the information comprises writing a first pointer from the host to the SAR queue; and

transferring the first cell payload comprises writing a first cell payload from the SAR to a first buffer in the host in response to the first pointer in the SAR queue.

12. (ORIGINAL) The method of claim 11 wherein writing the first cell payload from the SAR to the host in response to the first pointer in the SAR queue comprises activating a first host buffer descriptor in response to the first pointer in the SAR queue and writing the first cell payload from SAR to the first buffer in the host in response to activating the first host buffer descriptor.

13. (ORIGINAL) The method of claim 12 wherein the first host buffer descriptor is associated with the first buffer in the host and the first pointer indicates the first host buffer descriptor.

14. (ORIGINAL) The method of claim 13 further comprising:

activating a second host buffer descriptor in response to writing the first cell payload from the SAR to the first buffer in the host; and

writing a second cell payload from the SAR to a second buffer in the host in response to activating the second host buffer descriptor.

15. (ORIGINAL) The method of claim 11 further comprising writing a second pointer from the SAR to the host queue in response to transferring the first cell payload to the host to indicate that transfer of the first cell payload is complete.

16. (ORIGINAL) The method of claim 15 wherein the second pointer indicates the first host buffer descriptor that is associated with the first buffer in the host.

17. (CURRENTLY AMENDED) An Asynchronous Transfer Mode (ATM) system comprising:

a Segmentation and Re-assembly (SAR) queue configured to store information from a host wherein the host is configured to write to the SAR queue to indicate where the host is reading from a host queue; and

a SAR circuit configured to write to the host to indicate where the SAR circuit is reading from the SAR queue and to transfer a first cell payload between the host and the SAR circuit in response to the information in the SAR queue.

18. (ORIGINAL) The ATM system of claim 17 wherein the SAR circuit is configured to write to the host to indicate where the SAR is writing to a host queue.

19. (ORIGINAL) The ATM system of claim 18 wherein the SAR queue is configured to indicate if the information in the SAR queue has been processed.

20. (ORIGINAL) The ATM system of claim 19 wherein the information comprises a first pointer and the SAR circuit is configured to read a first cell payload from a first buffer in the host in response to the first pointer in the SAR queue.

21. (ORIGINAL) The ATM system of claim 20 wherein the SAR circuit includes a first SAR buffer descriptor and the SAR circuit is configured to activate the first SAR buffer descriptor in response to the first pointer in the SAR queue and to read the first cell payload from the first buffer in the host in response to activating the first SAR buffer descriptor.

22. (ORIGINAL) The ATM system of claim 21 wherein the first SAR buffer descriptor is associated with the first buffer in the host and the first pointer indicates the first SAR buffer descriptor.

23. (ORIGINAL) The ATM system of claim 22 wherein the SAR circuit includes a second SAR buffer descriptor and the SAR circuit is configured to activate the second SAR buffer descriptor in response to reading the first cell payload from the first buffer in the host and to read a second cell payload from a second buffer in the host in response to activating the second SAR buffer descriptor.

24. (ORIGINAL) The ATM system of claim 20 wherein the SAR circuit is configured to write a second pointer to the host queue in response to reading the first cell payload to indicate that transfer of the first cell payload is complete.

25. (ORIGINAL) The ATM system of claim 24 wherein the second pointer indicates a first host buffer descriptor that is associated with the first buffer.

26. (ORIGINAL) The ATM system of claim 19 wherein the information is a first pointer and the SAR circuit is configured to write a first cell payload a first buffer in the host in response to the first pointer in the SAR queue.

27. (ORIGINAL) The ATM system of claim 26 wherein the host includes a first host buffer descriptor and the SAR circuit is configured to activate the first host buffer descriptor in response to the first pointer in the SAR queue and to write the first cell payload to the first buffer in the host in response to activating the first host buffer descriptor.

28. (ORIGINAL) The ATM system of claim 27 wherein the first host buffer descriptor is associated with the first buffer in the host and the first pointer indicates the first host buffer descriptor.

29. (ORIGINAL) The ATM system of claim 28 wherein the SAR circuit is configured to write a second pointer from the SAR to the host queue in response to transferring the first cell payload to the host to indicate that transfer of the first cell payload is complete.

30. (ORIGINAL) The ATM system of claim 29 wherein the second pointer indicates the first host buffer descriptor that is associated with the first buffer in the host.

31. (ORIGINAL) The ATM system of claim 19 further comprising the host wherein the host is configured to write to the SAR to indicate where the host is reading from a host queue and where the host is writing to the SAR queue.

32. (ORIGINAL) The ATM system of claim 31 wherein the host is configured to indicate if the information in the host queue has been processed.

33. (ORIGINAL) The ATM system of claim 32 wherein the SAR circuit includes a first SAR buffer descriptor and the host includes a first host buffer descriptor and the SAR circuit and host are configured to mirror the first host buffer descriptor and the first SAR buffer descriptor.